This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-16 (canceled).

Claim 17 (new):A non-volatile memory structure comprising:

a substrate;

a plurality of gate dielectric layers disposed on the substrate, wherein at least one hetero element is planted on the top layer of the gate dielectric layers so as to provide an increased electron trapping density in the gate dielectric layers;

a gate electrode layer formed on the top of the gate dielectric layers; and a source/drain electrode formed at the substrate on both sides of the gate dielectric layer.

Claim 18 (new): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers including a first oxide layer, a nitride layer, and a second oxide layer.

Claim 19 (new): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers comprises at least one layer made of silicon carbide.

Claim 20 (new): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers comprises at least one layer made of aluminum oxide (Al2O3).

Claim 21 (new): the non-volatile memory structure as claimed in claim 17, wherein the at least one hetero element is selected from a group consisting of germanium, silicon, nitrogen, or oxygen.

Claim 22 (new): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers including a first silicon dioxide layer, a silicon nitride layer, and a second silicon dioxide layer.

Claim 23 (new): a non-volatile memory structure comprising:

a plurality of gate dielectric layers disposed on a substrate, said gate dielectric layers comprising a first dielectric layer formed on the substrate, a second dielectric layer formed on said first dielectric layer, and a third dielectric layer formed on said second dielectric layer, said first dielectric layer and said second dielectric layer are different materials, wherein at least one hetero element is planted on the third dielectric layer for increasing electron trapping density in the gate dielectric layers;

a gate electrode layer formed on said plurality of gate dielectric layers; and

a source/drain electrode formed at said substrate on both sides of said plurality of gate dielectric layers.

Claim 24 (new): the non-volatile memory structure as claimed in claim 23, wherein said first dielectric layer including a first oxide layer and said second dielectric layer comprising a nitride layer.

Claim 25 (new): the non-volatile memory structure as claimed in claim 23, wherein said first dielectric layer and said third dielectric layer are same material.

Claim 26 (new): the non-volatile memory structure as claimed in claim 23, wherein said at least one hetero element is germanium.

Claim 27 (new): the non-volatile memory structure as claimed in claim 23, wherein said at least one hetero element is silicon.

Claim 28 (new): the non-volatile memory structure as claimed in claim 23, wherein the gate dielectric layers comprises at least one layer made of silicon carbide.

Claim 29 (new): the non-volatile memory structure as claimed in claim 23, wherein the gate dielectric layers comprises at least one layer made of aluminum oxide (Al2O3).

Claim 30 (new): the non-volatile memory structure as claimed in claim 23, wherein said at least one hetero element is selected from a group consisting of germanium, silicon, nitrogen, or oxygen.

Claim 31 (new): the non-volatile memory structure as claimed in claim 23, wherein the gate dielectric layers including a first silicon dioxide layer, a silicon nitride layer, and a second silicon dioxide layer.

Claim 32 (new): a non-volatile memory structure comprising:

a plurality of gate dielectric layers disposed on a substrate, said gate dielectric layers comprising a first dielectric layer formed on the substrate, a second dielectric layer formed on said first dielectric layer, and a third dielectric layer formed on said second dielectric layer, said first dielectric layer and said second dielectric layer are different materials, wherein at least one hetero element is planted into said second dielectric layer for increasing electron trapping density;

a gate electrode layer formed on said plurality of gate dielectric layers; and

a source/drain electrode formed at said substrate on both sides of said plurality of gate dielectric layers.

Claim 33 (new): the non-volatile memory structure as claimed in claim 32, further comprising a fourth dielectric layer.